Amendment to the Specification:

Please delete the paragraph beginning at page 1 line 4, which starts with "**TECHNICAL FIELD**" and ends at page 1 line 7 with "... resetting a microprocessor system."

Please add the following new paragraph after the title:

CROSS-REFERENCE TO RELATED APPLICATIONS

This is a National Stage Application of International Patent Application No. PCT/PL 03/00058, with an international filing date of June 17, 2003, which is based on Polish Patent Application No. P-354827, filed July 1, 2002.

Please replace the heading at page 1 line 8: "**BACKGROUND ART**" with the following new heading and paragraphs:

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a circuit for detection of internal microprocessor watchdog device execution and a method for resetting a microprocessor system.

2. Brief Description of the Background of the Invention Including Prior Art

Please replace the heading at page 2 line 25: "**DISCLOSURE OF INVENTION**" with the following new paragraph:

SUMMARY OF THE INVENTION

1. Purposes of the Invention

It is an object of this invention to provide a circuit for detection of watchdog device execution more efficient than know circuits.

This and other objects and advantages of the present invention will become evident from the description which follows.

2. Brief Description of the Invention

Please add the following new paragraph at page 3 after line 26 (immediately preceding the section **BRIEF DESCRIPTION OF DRAWINGS**):

The novel features which are considered as characteristic for the invention are set forth in the appended claims. The invention itself, however, both as to its construction and its method of operation, together with additional objects and advantages thereof, will be best

understood from the following description of specific embodiments when read in connection with the accompanying drawings.

Please replace the heading at page 4 line 5: "**BEST MODE FOR CARRYING OUT THE INVENTION**" with the following new heading: **DESCRIPTION OF THE INVENTION AND PREFERRED EMBODIMENT**

Please amend the paragraph starting at page 5, line 24, by adding the numeral "33" at page 6, line 7, after the words "to a low state" and before the words "(a logic "0")", as follows:

Fig. 2 presents a plot of a System_reset signal 26 (triggered by the system reset circuit 19), a plot of the /Q signal 27 (triggered by the flip-flop 12), a plot of the WDOG_PIO signal 31 (triggered by the CPU 6) and a plot of the CPU_nreset signal 45 (triggered by the internal watchdog 2). When the reset signal 21 is generated, the whole system, including the CPU 6, is reset. The reset of the CPU 6 results in setting the input/output line 18 to a high impedance state. The WDOG_PIO input/output line 11 of the CPU 6 is also set to the high impedance state, and through the resistor 10 it is set to a high state 32. After the reset procedure is finished 22, the CPU 6 executes a program that results in setting the WDOG_PIO input/output line 11 to a low state 33 (a logic "0") and performs further actions. The system starts its normal operation. If the system operation is disrupted, the watchdog 2 sends a reset signal 41 through the CPU_nreset output, which results in the reset of the CPU 6. Next, the CPU 6 sets the input/output lines 18 to a high impedance state. The WDOG_PIO input/output line 11 of the CPU 6 is also set to a high impedance state, and through the resistor 10 it is set to a high state 34. In the meantime, the reset signal becomes inactive 42. The change in state 34 of the WDOG_PIO input/output line 11 results in activation of the flip-flop 12. The output 13 of the flip-flop 12 is switched to a low state 28, thereby activating the system reset circuit 19, which results in activating at its output 20 a reset signal of a low state 23. This signal switches the output 13 of the flip-flop 12 to a high state 29, which results in deactivation system reset signal. After the system reset is finished 24, the CPU 6, executing the processor startup program, sets the WDOG_PIO input/output line 11 to a low state 35, enabling further system operation.

Please add the following new paragraphs at page 7 after line 4:

It will be understood that each of the elements described above, or two or more together, may also find a useful application in other types of methods for allocation of data differing from the types described above.

While the invention has been illustrated and described as embodied in the context of a method for allocation of data for images in operating memory, it is not intended to be limited to the details shown, since various modifications may be made without departing in any way from the spirit of the present invention.

Without further analysis, the foregoing will so fully reveal the gist of the present invention that others can, by applying current knowledge, readily adapt it for various applications without omitting features that, from the standpoint of prior art, fairly constitute essential characteristics of the generic or specific aspects of this invention.

What is claimed as new and desired to be protected by Letters Patent is set forth in the appended claims.